IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	: 10/726,922	Confirmation No.	: 8797
Applicants	: PATTANAYAK, Deva; XU, Robert		
Filed	: December 2, 2003		
T.C./A.U.	: 2815		
Examiner	: FENTY, Jesse		
Title	: Closed Cell Trench Metal-Oxide-Semiconductor Field Effect Transistor		
Docket No.	: VISH-8728		

DECLARATION OF PRIOR INVENTION
TO OVERCOME CITED PATENT OR PUBLICATION
37 C.F.R. § 131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants, Deva Pattanayak and Robert Xu, respectfully assert that the invention as claimed in U.S. Patent Application No. 10/726,922, filed December 2, 2003, was completed in the United States at a date prior to April 7, 2003, that is the effective date of the prior art, U.S. Patent Application No. 2004/0195618, that was cited by the Examiner. To establish the date of

completion of the invention of this application, Applicants have attached a copy of the Patent Disclosure submitted by the Applicant Deva Pattanayak to the Chief Executive Office, King Owyang, for the Assignee, Vishay Siliconix. From the Patent Disclosure document, it can be seen that the invention of the present application was reduced to practice at least by the data of November 19, 2002, which is a date earlier than the effective data of the reference.

Applicants hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: May 12, 2006 Deva Pattanayak

Deva Pattanayak

Dated: May 15, 2006 Robert Xu

Robert Xu

To:

King Owyang
CEO, Vishay Siliconix
Santa Clara, CA

From:
Deva N. Pattanayak
Director, Device Technology
Vishay Siliconix, Santa Clara, CA

Date: November 19, 2002

Subject: Patent Disclosure on PWM Optimized Closed Cell MOSFET

Basic Idea:

The gate drain overlap of closed cell TMOSFETs are selectively blocked by the body region (which is connected to the source) to reduce the gate to drain capacitance of the closed cell TMOSFEts. This increases the gate to source capacitance and decreases the channel component of the resistance because all the trenches in a closed cell structure are connected. This will enable closed cell structures to have lower Qgd/Qgs ratio needed for the low side synchronous MOSFET device. The low Qgd design can be used also for the high side switching device with lower RdsonA value for the same Qgd/A value thus improving the figure of merit Rson*Qgd.

Description of the Invention:

We start with the top view of a closed cell TMOSFET shown in Figure (1).

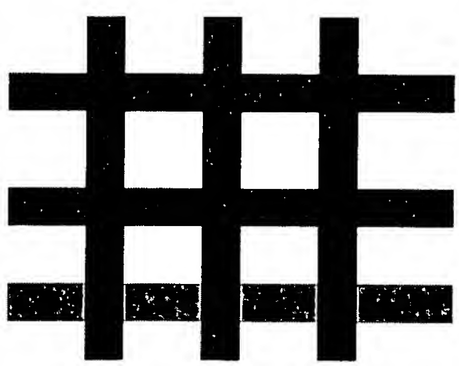


Figure (1) Closed Cell Trench Topology (Top View) .

The trenches are shown in blue and are all connected. The device that we will describe can be realized in many ways. Here we describe one simple way to accomplish the structure described in the basic idea section.

We use a photo-resist mask to block the columns of trenches and implant through the trench bottom N type dopant, say Arsenic through the open trenches as shown below

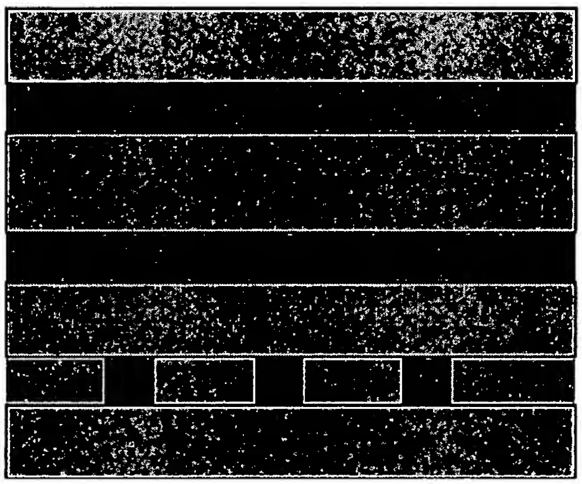
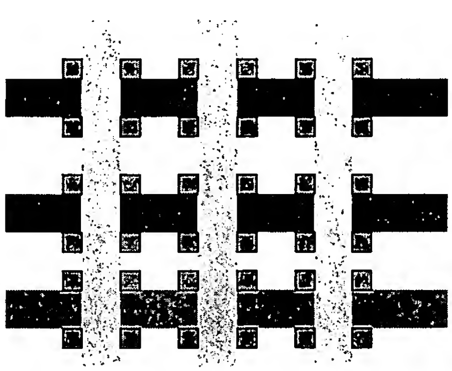


Figure (2) Vertical Trenches covered with Photoresist

The red regions denote the photoresist regions. The blue open trench regions get the trench bottom implant.

We then remove the photo-resist layer and complete the regular steps of the trench MOSFET process. In this version the Body fully covers the trench bottom of the horizontal trenches and the vertical trench bottoms are connected through the trench bottom implant to the N epitaxial layer over N+-substrate which forms the drain region.

The top view of the closed cell structure id shown in Figure (3).



Figure(3) Closed Cell PWM optimized TMOSFET:

The red regions denote the source. Orange Trench bottoms are inverted when the gate to source is above threshold voltage and the channel current flows into the drain through the blue inverted channels and then to the drain through the implanted regions that connects the blue channel to the drain via the trench bottom accumulation regions. Thus the orange colored trenches participate in lowering the overall channel resistance, but does not increase the Qgd. They however increase the Qgs. Thus these structures can be candidate for the low side MOSFET in the DC-DC converter as synchronous MOSFET having low Rds and low Qgd/Qgs ratio.

We show a cross section of the closed cell along the horizontal direction(A-A) below:

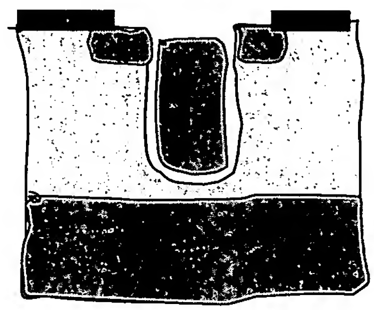


Figure (4) Source to Source Conduction Channel : Current flows from this channel into the adjacent MOSFET and into the Drain.

The cross section of the closed cell along the vertical direction (B-B) is shown below:

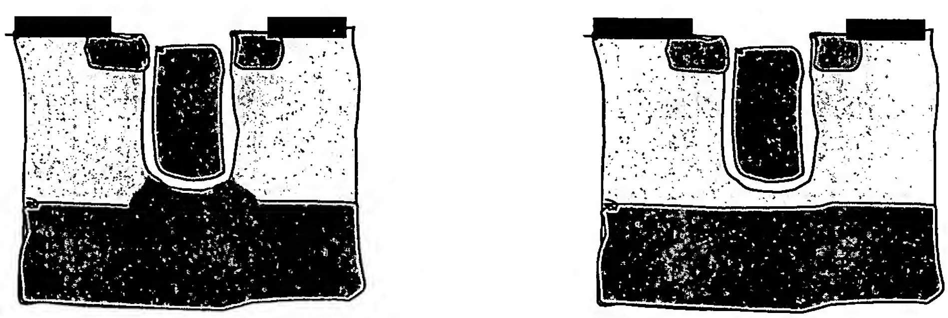
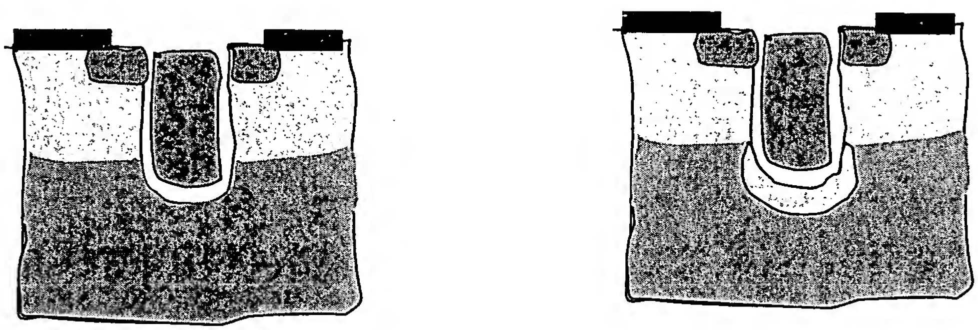


Figure (5) Trench Bottom implanted Trench (Open Bottom) is connected with the channel of adjacent non-implanted Trench Bottom (Closed Bottom) MOSFET. Connection shown symbolically:

The channel portions of the orthogonal sections of the TMOSFET are connected which is shown symbolically in Figure (5). The source current from the adjacent closed bottom trench MOSFET will pass

through the connected open bottom trench MOSFET. The gate to channel capacitance of the closed bottom Trench MOSFET will appear across the gate to source terminal, thus increasing the Cgs and decreasing Cgd. The parallel channel current path from the drain to the source of the closed bottom trench will reduce the total channel resistance. Therefore the figure of merit (rdson*Qgd) of this three dimensional TMOSFET structure will be lower than the traditional stripe geometry.

Other embodiment of this idea is to reduce the body diffusion so that one realizes regular open bottom trench structures and implant Boron to close the bottom of the orthogonal trenches. The resulting cross sections are shown below in Figure (6).



Figure(6) Normal Trench Bottom MOSFET   Boron Implanted Trench Bottom MOSFET

Once again the gate to drain capacitance in the Boron implanted Trench Bottom MOSFET structure is transferred to the gate to source capacitance. Just like the previous structure, the total Cgd/Cgs ratio for this closed cell structure is decreased and the Rdson*Qgd figure of merit is reduced.

Obviously one can selectively use the trench bottom implant and impact the capacitance and resistance values by this method.

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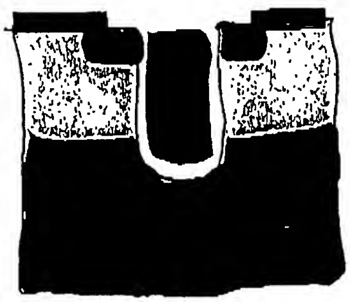

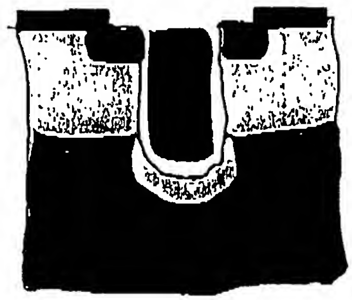

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Inventor: DPattanayak (Deva N. Pattanayak) Date: Nov 19, 2002

Witnessed and understood by: Kyle Terrill Date: 11/19/02

Witnessed and understood by: Jacek Korec Date: 11/19/02

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